DESIGN OF UNIVERSAL GATES USING MATLAB & MICROWIND

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ABSTRACT

According to Moore's Law, the no of transistors in an IC chip doubles every 18 months. This leads in increase in power density. Hence in modern power circuits, the main factor of the circuit efficiency is power efficiency. Due to scaling, leakage power accounts for an increasingly large portion of the total power consumption in deep submicron technologies. In this article, we proposed a methodology to find the problems occurring while scaling it into small size with some factor. We have simulated the inverter circuit using CMOS in MATLAB, DSCH3 .where we can vary the physical dimensions of the MOSFET. The outputs were observed and the time delay was calculated. The above results showed that, as we go on reducing the size, the performance enhances. Due to some limitations, the CMOS were facing some of the problems like Drain induced barrier lowering (DIBL), Velocity Saturation, Punch through, Oxide Breakdown, Channel length modulation.Hence due to the above factors, FinFET technology has proposed as an alternative to deep submicron bulk CMOS. FinFET is likely to meet the performance requirements in the sub-20nm gate length regime. FinFET will replace the traditional MOSFET due to its better performance in sub 20nm regime and also it has excellent control over the problems faced by the Traditional CMOS.The objective is to simulate the inverter circuit using CMOS through MATLAB,. The merits of small scale are also discussed. The future work is to replace the Bulk-CMOS with the nano-CMOS and make the system faster. This includes SD-RAM, Processor, logic circuits, and switches, and also where we can implement these applications. FinFET being one of the nano device is the better option among all the devices because of smaller size among all the above. FinFET can overcome all the Problems caused by scaling the MOSFET into the nano regime.Wide FinFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the FinFETs double gates allows significant reduction in leakage current.

KEYWORDS: CMOS, Drain Gate, Source, MATLAB

INTRODUCTION

Metal-Oxide-Semiconductor Field Effect Transistor is a three terminal device used for a variety of applications as per the requirement in different fields of electronics. It is used for amplifying or switching electronic signals. The basic principle of the device was first proposed by Julius Edgar Lilienfeld in 1925. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type and is accordingly called an nMOSFET or a pMOSFET (also commonly nMOS, pMOS). Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM, recently started using a chemical compound (bond, NOT a mixture) of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETs.
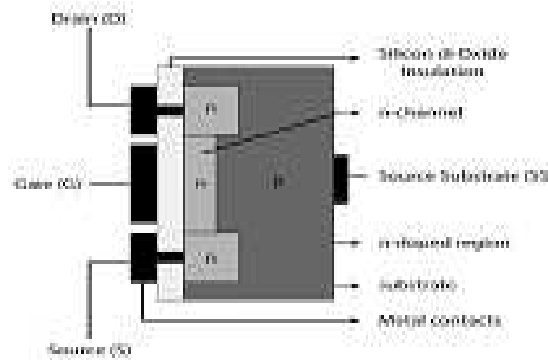
CONSTRUCTION

Figure 1: (Structure of MOSFET)

The basic construction of the n-channel enhancement-type MOSFET is provided in. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally external control of its potential level. The source and drain terminals are again connected through metallic contacts to n-doped regions. This is the primary difference between the constructions of depletion-type and enhancement-type MOSFETs -the absence of a channel as a constructed component of the device. The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

OPERATION

A traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a P-type semiconductor (with NA the density of acceptors, p the density of holes; p = NA in neutral bulk), a positive voltage, VGB, from gate to body. The creates a depletion layer by forcing the positively charged holes away from the gateinsulator/ semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If VGB is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator. Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region.Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage. This structure with P-type body is the basis of the N-type MOSFET, which requires the addition of an N-type source and drain regions.

SIMULATION RESULTS

Simulation of CMOS Inverter Logic Circuit Using MATLAB

Simulation of inverter circuit was carried out using CMOS through MATLAB software. And output was observed. NOT gate and NAND gate was designed through MATLAB
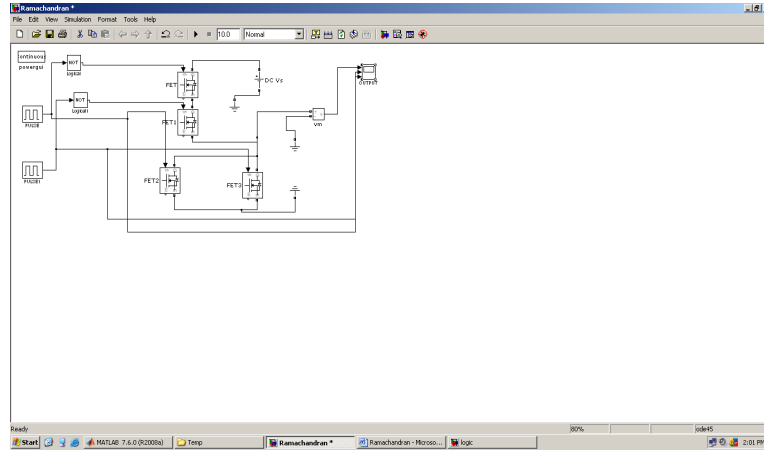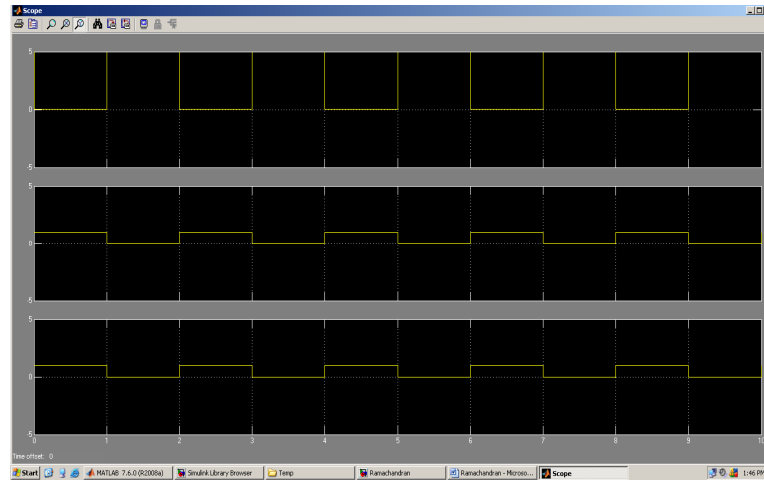
Figure 2: Basic Logic Circuit

Figure 3: Basic Logic Circuit Simulation Output

BOOLEAN FUNCTIONS: NAND GATE IS A UNIVERSAL GATE

To prove that any Boolean function can be implemented using only NAND gates, we will show that the AND, OR, and NOT operations can be performed using only these gates
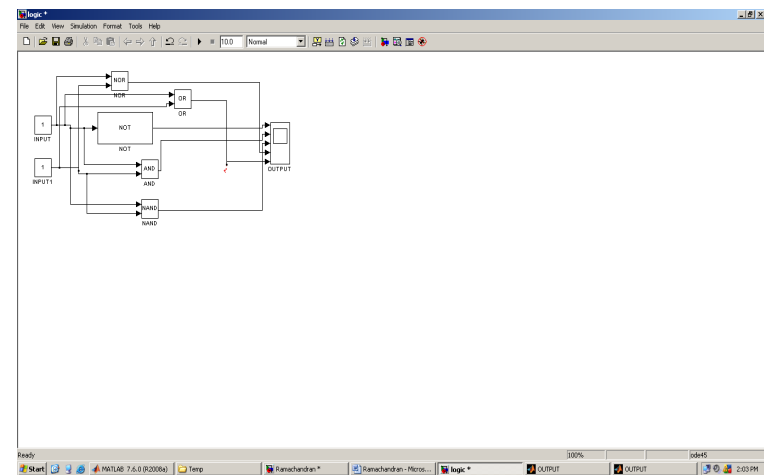

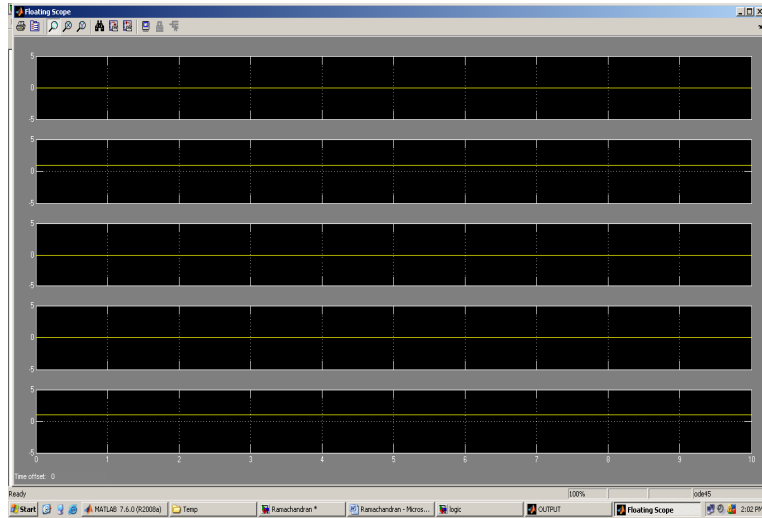**Figure 4: Universal Gates Circuits**
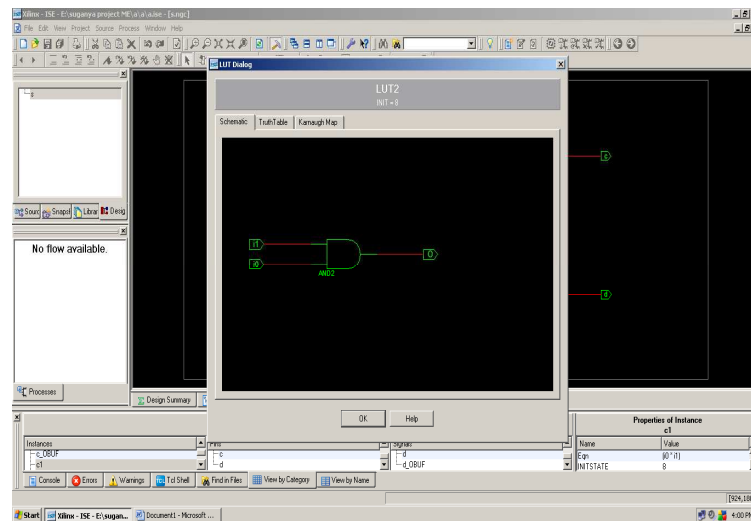
Figure 5: Universal Gates Circuits Simulation Output

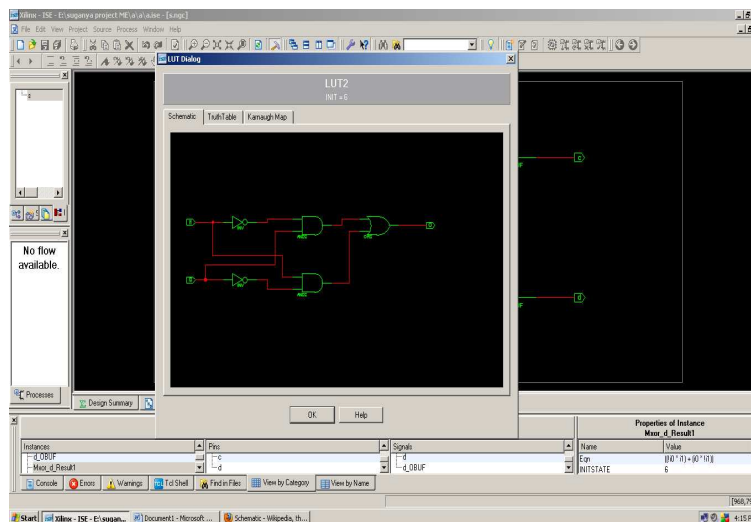

Figure 6: Basic AND, NOT and OR Gates

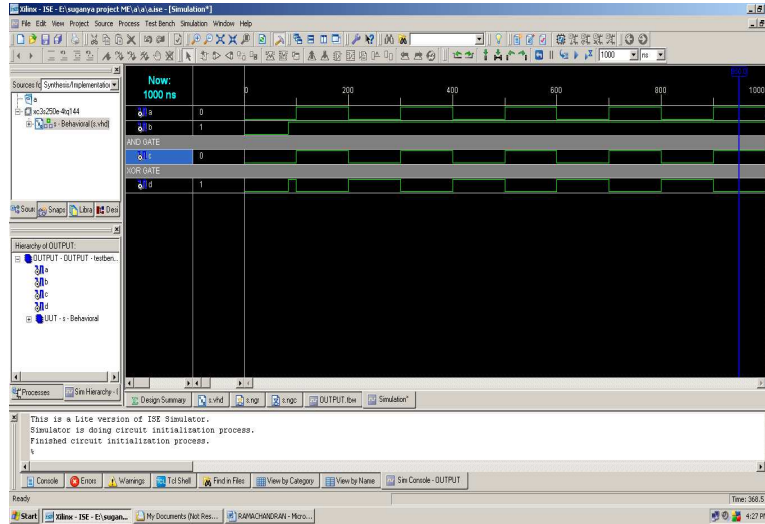**Figure 7: Basic AND, NOT and OR Gates Universal ie NAND or NOR Gates**

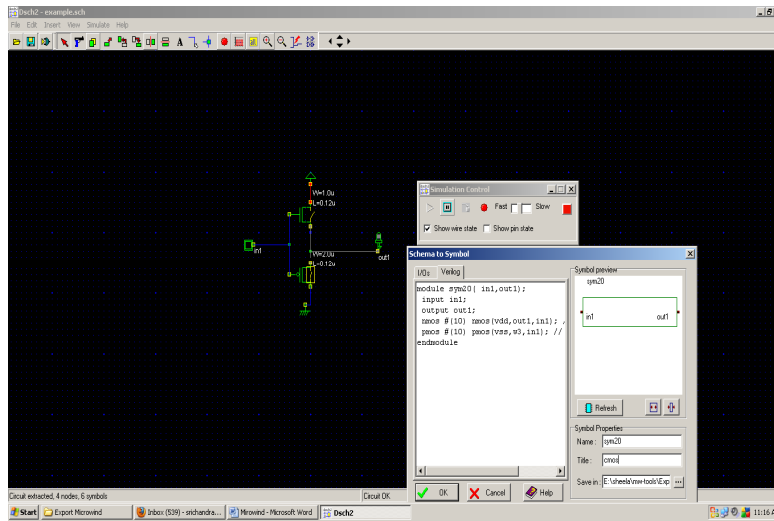**Figure 8: Simulation Output: Universal & Combinational Gates**
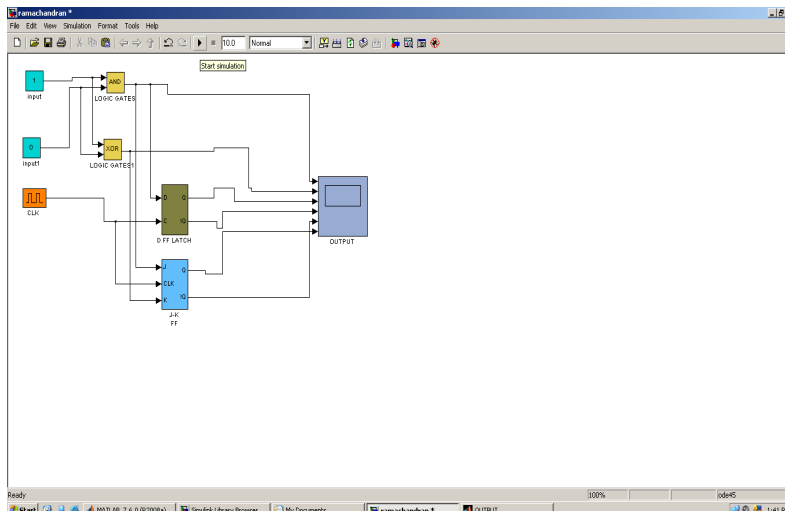

Figure 9: CMOS Inverter Circuits

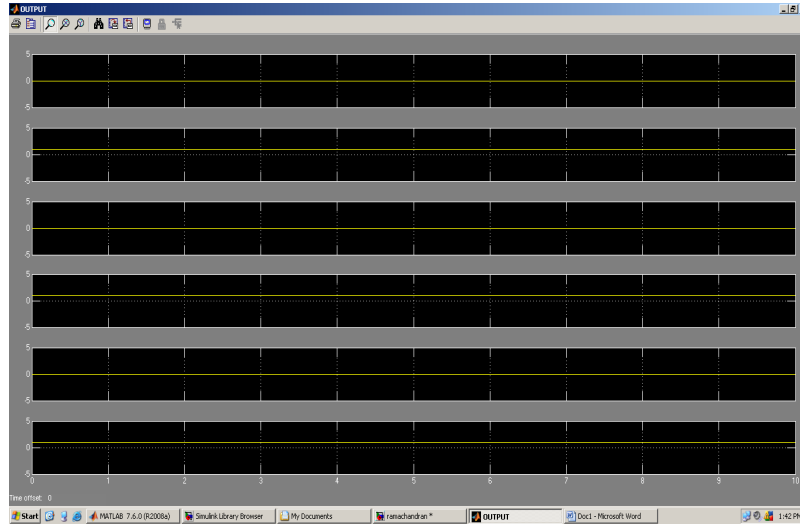**Figure 10: Design D Flip Flop & JK Flip Flop**

Figure 11: Design D Flip Flop & JK Flip Flop Simulations

CONCLUSIONS

We hereby conclude that, the simulations of CMOS logic inverter using MATLAB, DSCH3 Each nano-transistor is consuming very less power in comparison to the bulk ones. And hence in the IC chip consisting of more no of MOSFET will consume less power and give more efficiency.

Downsizing of MOSFET results in

- Reduce capacitance.

- Reduce switch time of MOSFET.

- Reduce power consumption.

- Increase no of transistors.

- Increase functionality.

- Parallel Processing.

- Increase Circuit Operation Speed.

Thus downscaling of Si devices is very essential and it very much enhances the performance of the device in terms of power consumption, speed, etc.

And as per Moore's Law, the no of transistors to be fabricated in an IC chip increases exponentially. Thus, device can operate faster with more no of transistors. FinFET due to its fast operation, low power consumption, smaller size so that more no of transistors can be accommodate in a single IC chip. Being very fast operating device, low power consuming, and very tiny, the device is best option for our future applications. The no of transistor fabricated in single IC will be very large in no., if we use FinFET.

APPLICATIONS

Some of the nano-CMOS are DG-MOSFET, FinFET, DG-FinFET, ultra-small MOSFETs, SiGe HBTs. These can be used for different applications in the world of electronics, such as SD-RAM and Processors, etc. and also in mobile

technology. It is also used in Low Power Applications of CMOS circuits. Hence, the Nano-Technology based MOSFET replace the bulk CMOS and will make the computer-era faster and more reliable. It will bring revolution in the world of communication and electronics, as everything is digitalized and depends on transistors. Even a small digital clock needs timer circuits for its operation and also a computer processor, RAM etc.; they too need transistor for operation. FinFET advantages over bulk MOS are, it is very small in size, low power consuming, fast operating, and it also has same fabrication process as a MOSFET. FinFET being very small in size, more no can be fabricated in a single IC chip. And works are going on to make the transistor in nano range so as to check some of the problems caused by small scaling such as Power Density, temperature etc.

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